

a

# Precision Low Noise JFET Operational Amplifiers

## Preliminary Technical Data

### AD8510/AD8512/AD8513

#### FEATURES

- Low Offset Voltage: 400  $\mu$ V max
- Low TcVos: 2  $\mu$ V/ $^{\circ}$ C typ
- Low input bias current: 30pA max.
- Dual-Supply Operation:  $\pm$ 5V to  $\pm$ 15V Volts
- Low Noise: 8 nV/ $\sqrt{\text{Hz}}$
- Fast settling: 10V step to 0.01% in 600ns
- No Phase Reversal
- Unity Gain Stable

#### APPLICATIONS

- Instrumentation
- Multi-pole filters
- Precision current measurement
- Photo-diode amplifiers
- Sensors
- Audio

#### GENERAL DESCRIPTION

The AD8510, AD8512 and AD8513 are single, dual and quad precision JFET amplifiers featuring low offset voltage, low input bias current and low input voltage and current noise.

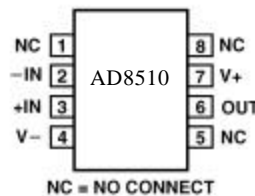
The combination of low offsets, low noise and very low input bias currents make these amplifiers especially suitable for high impedance sensor amplification and precise current measurements using shunts. Unlike many older JFET amplifiers these parts do not suffer from output phase reversal when input voltages exceed the maximum common mode voltage range.

The AD8510, AD8512 and AD8513 are specified over the extended industrial ( $-40^{\circ}$  to  $+125^{\circ}$ C) temperature range. The AD8510, single, and AD8512, dual, are available in the 8 lead MSOP and narrow SOIC surface mount packages. The

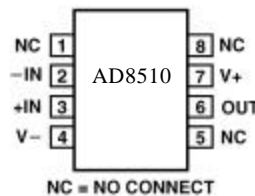
AD8513 is available in the 14 lead TSSOP and narrow SOIC packages. MSOP and TSSOP versions are available in tape and reel only.

#### PIN CONFIGURATIONS

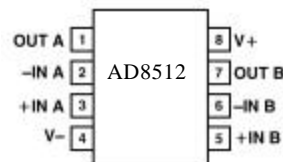
8-Lead MSOP (RM-8)



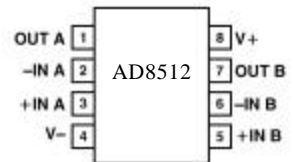
8-Lead SO (R-8)



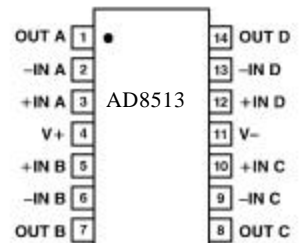
8-Lead MSOP (RM-8)



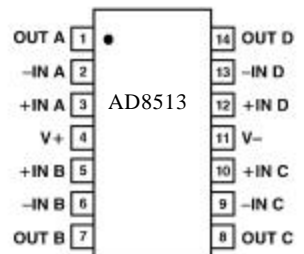
8-Lead SO (R-8)



14-Lead TSSOP (RU-14)



14-Lead SO (R-14)



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, PO Box 9106, Norwood, MA 02062-9106, USA

Tel: 617/329-4700  
Fax: 617/326-8703

World Wide Web Site: <http://www.analog.com>  
© Analog Devices, Inc., 2001

# PRELIMINARY TECHNICAL DATA

## AD8510/AD8512/AD8513

### ELECTRICAL CHARACTERISTICS ( $V_S = \pm 5V$ , $V_{CM} = 0V$ , $T_A = +25^\circ C$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage (A Grade)	$V_{OS}$	$-40^\circ < T_A < +125^\circ C$			1	mV
Offset Voltage (B Grade)	$V_{OS}$	$-40^\circ < T_A < +125^\circ C$			1.8	mV
					.4	mV
					0.8	mV
Input Bias Current	$I_B$	$-40^\circ < T_A < +85^\circ C$			30	pA
		$-40^\circ < T_A < +125^\circ C$			2	nA
					30	nA
Input Offset Current	$I_{OS}$	$-40^\circ < T_A < +85^\circ C$			25	pA
		$-40^\circ < T_A < +125^\circ C$			1.6	nA
					13	nA
Input Voltage Range			-4		3.2	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.5V$ to $3V$	86			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ $V_O = -3V$ to $3V$	150	200		V/mV
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$			3	10	$\mu V/^\circ C$
Offset Voltage Drift (B Grade)	$\Delta V_{OS}/\Delta T$			2	10	$\mu V/^\circ C$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ C < T_A < +125^\circ C$	3.5			V
			3.4			V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ C < T_A < +125^\circ C$			-4	V
					-3.4	V
Output Current	$I_{OUT}$		$\pm 25$	$\pm 35$		mA
Closed Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}$ , $A_V = 1$		tbd		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$	86			dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0V$ $-40^\circ < T_A < +125^\circ C$		1.8	3	mA
					4	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		20		V/ $\mu s$
Gain Bandwidth Product	GBP			7.5		MHz
Settling Time	$t_s$	to 0.01%, 0V to 4V step		.3		$\mu s$
THD+Noise	THD+N			.0001		%
Phase Margin	$\phi_o$			60		degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		8		nV/ $\sqrt{\text{Hz}}$
Voltage Noise Density	$e_n$	$f = 10\text{ kHz}$		8		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$

# PRELIMINARY TECHNICAL DATA

## AD8510/AD8512/AD8513

### ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15.0V$ , $V_{CM} = 0V$ , $T_A = +25^\circ C$ unless otherwise noted)

Parameter	Symbol	Conditions	A Grade			Units
			Min	Typ	Max	
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage (A Grade)	$V_{OS}$	$-40^\circ < T_A < +125^\circ C$			1	mV
Offset Voltage (B Grade)	$V_{OS}$	$-40^\circ < T_A < +125^\circ C$			1.8	mV
					.4	mV
					0.8	mV
Input Bias Current	$I_B$	$-40^\circ < T_A < +85^\circ C$			30	pA
		$-40^\circ < T_A < +125^\circ C$			2	nA
					30	nA
Input Offset Current	$I_{OS}$	$-40^\circ < T_A < +85^\circ C$			25	pA
		$-40^\circ < T_A < +125^\circ C$			1.6	nA
					13	nA
Input Voltage Range			-13.5		13	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12.5V$ to $12.5V$	86			dB
Large Signal Voltage Gain	$A_{VO}$	$V_O = -13V$ to $13V$ , $R_L = 2\text{ k}\Omega$ , $V_{CM} = 0V$	150	200		V/mV
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$			3	10	$\mu V/^\circ C$
Offset Voltage Drift (B Grade)	$\Delta V_{OS}/\Delta T$			2	10	$\mu V/^\circ C$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1mA$	13.5			V
		$I_L = 10mA$	13			V
		$-40^\circ C$ to $+125^\circ C$	12			V
Output Voltage Low	$V_{OL}$	$I_L = 1mA$			-13.5	V
Output Voltage High	$V_{OL}$	$I_L = 10mA$			-13	V
		$-40^\circ C$ to $+125^\circ C$			-12	V
Output Current	$I_{OUT}$			$\pm 50$		mA
Closed Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}$ , $A_V = 1$		tbd		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$	86			dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0V$		1.8	3.5	mA
		$-40^\circ < T_A < +125^\circ C$			4.5	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		20		V/ $\mu s$
Gain Bandwidth Product	GBP			7.5		MHz
Settling Time	$t_s$	to 0.01%, 0V to 10V step		.9		$\mu s$
THD+Noise	THD+N			.0001		%
Phase Margin	$\phi_o$			60		degrees

# PRELIMINARY TECHNICAL DATA

## AD8510/AD8512/AD8513

NOISE PERFORMANCE				
Voltage Noise Density	$e_n$	f=1kHz	8	nV/ $\sqrt{\text{Hz}}$
Voltage Noise Density	$e_n$	f=10kHz	8	nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	f=1kHz	0.015	pA/ $\sqrt{\text{Hz}}$

### ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply voltage .....	±18V
Input Voltage.....	±Vs
Output Short-Circuit Duration to Gnd <sup>2</sup> ... Observe Derating Curves	
Storage Temperature Range	
R, RM, RU Package .....	-65°C to +150°C
Operating Temperature Range	
AD8510/AD8512/AD8513.....	-40°C to +125°C
Junction Temperature Range	
R, RM, RU Package .....	-65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec).....	+300°C
Electrostatic Discharge (HBM).....	2000V

Package Type	$\theta_{JA}$	$\theta_{JC}$	Units
8-Pin MSOP (RM)	210	45	°C/W
8-Pin SOIC (R)	158	43	°C/W
14-Pin TSSOP (RU)	158	43	°C/W
14-Pin SOIC (R)	158	43	°C/W

### NOTES

<sup>1</sup> Absolute maximum ratings apply at 25°C, unless otherwise noted.

<sup>2</sup>  $\theta_{JA}$  is specified for the worst case conditions, i.e.,  $\theta_{JA}$  is specified for device soldered in circuit board for surface mount packages.

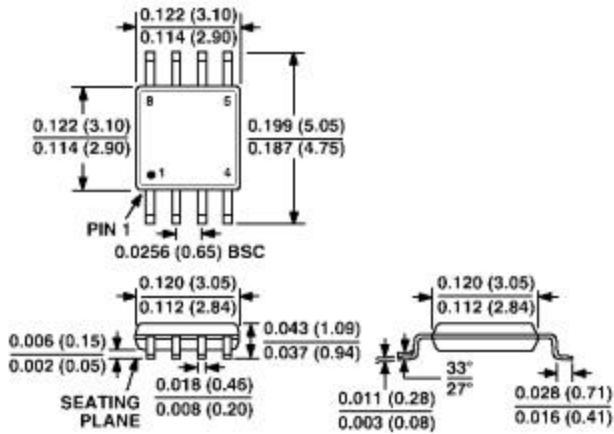
### ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Marking Code
AD8510ARM	-40°C to +125°C	8-Pin MSOP	RM-8	B7A
AD8510AR	-40°C to +125°C	8-Pin SOIC	R-8	
AD8510BR	-40°C to +125°C	8-Pin SOIC	R-8	
AD8512ARM	-40°C to +125°C	8-Pin MSOP	RM-8	B8A
AD8512AR	-40°C to +125°C	8-Pin SOIC	R-8	
AD8512BR	-40°C to +125°C	8-Pin SOIC	R-8	
AD8513ARU	-40°C to +125°C	14-Pin TSSOP	RU-14	
AD8513AR	-40°C to +125°C	14-Pin SOIC	R-14	

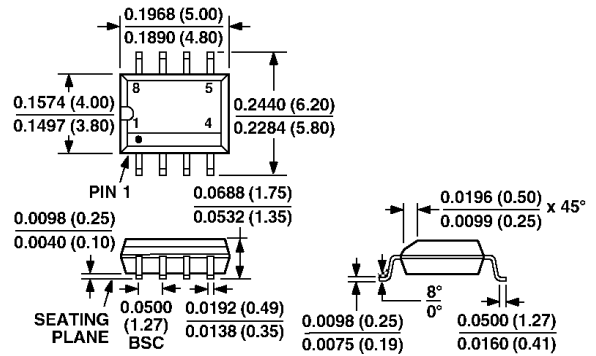
# PRELIMINARY TECHNICAL DATA

## AD8510/AD8512/AD8513

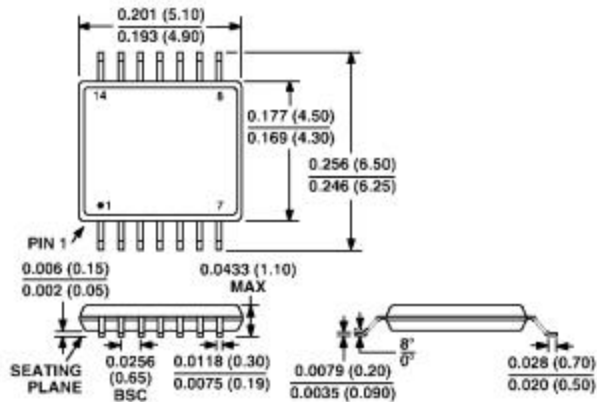
**8-Lead SOIC  
(RM-8)**



**8-Lead SO  
(R-8)**



**14-Lead TSSOP  
(RU-14)**



**14-Lead SO  
(R-14)**

